IN THE CLAIMS

1. (Original) A semiconductor memory device comprising:

a voltage level detector configured to generate a power-up signal;

a ready/busy driver controller configured to generate a busy enable signal in response to the power-up signal; and

a ready/busy driver that is responsive to the busy enable signal.

2. (Original) The device of claim 1, further comprising a command register cooperatively coupled to the ready/busy driver controller.

3. (Original) The device of claim 2, wherein the command register comprises:

a program command register configured to provide a program busy signal to the ready/busy driver controller; and

an erase command register configured to provide an erase busy signal to the ready/busy driver controller.

4. (Original) The device of claim 3, wherein the program busy signal indicates that the memory device is in a program mode.

5. (Original) The device of claim 3, wherein the erase busy signal indicates that the memory device is in an erase mode.

6. (Original) The device of claim 1, wherein the ready/busy driver controller comprises:

a control signal generator configured to generate a first and a second control signal in response to the power-up signal; and

a level shifter configured to generate the busy enable signal in response to the first and second control signals.

7. (Original) The device of claim 1, wherein the ready/busy driver comprises:

a ready/busy pin;

an open drain driver configured to set a voltage at the ready/busy pin in response to the busy enable signal; and

a pull up load connected to the ready/busy pin.

8. (Original) The device of claim 7, wherein the memory device is in a busy state during a power-up period when the voltage at the ready/busy pin is at a low state.

9. (Original) The device of claim 8, wherein the memory device is in a ready state after the power-up period.

10. (Original) A method of accessing a semiconductor memory device comprising:

determining if an internal voltage has reached an operational voltage level;

accessing the semiconductor memory device when the internal voltage has reached an operational voltage level.

11. (New) A semiconductor memory device comprising:

a voltage level detector configured to generate a power-up signal;

a ready/busy driver controller configured to generate a busy enable signal in response to the power-up signal; and

a ready/busy driver that is responsive to the busy enable signal;

wherein the ready/busy driver controller comprises:

a control signal generator configured to generate a first and a second control signal in response to the power-up signal; and

a level shifter configured to generate the busy enable signal in response to the first and second control signals.

12. (New) A semiconductor memory device comprising:

a voltage level detector configured to generate a power-up signal;

a ready/busy driver controller configured to generate a busy enable signal in response to the power-up signal; and

a ready/busy driver that is responsive to the busy enable signal;

wherein the ready/busy driver controller comprises:

a ready/busy pin;

an open drain driver configured to set a voltage at the ready/busy pin in response to the busy enable signal; and

a pull up load connected to the ready/busy pin.

13. (New) The device of claim 12, wherein the memory device is in a busy state during a power-up period when the voltage at the ready/busy pin is at a low state.

14. (New) The device of claim 13, wherein the memory device is in a ready state after the power-up period.